1) What is the difference between Latch And Flip-flop?

The difference between latches and Flip-flop is that the latches are level triggered and flip-flops are edge triggered. In latches level triggered means that the output of the latches changes as we change the input and edge triggered means that control signal only changes its state when goes from low to high or high to low.

Latches are fast whereas flip-flop is slow.

3) State the De Morgan's Theorem?

De Morgan's Theorem stated two theorems:

1.The complement of a product of two numbers is the sum of the complements of those numbers.

(A. B)' = A' + B'

9) What are the basic Logic gates?

There are three basic logic gates-

AND gate.

OR gate.

NOT gate.

11) What are the applications of the octal number system?

The applications of the octal number system are as follows:

For the efficient use of microprocessors.

For the efficient use of digital circuits.

It is used to enter binary data and display of information.

12) What are the fundamental properties of Boolean algebra?

The basic properties of Boolean algebra are:

Commutative Property.

Associative Property.

Distributive Property.

14) What is meant by K-Map or Karnaugh Map?

K-Map is a pictorial representation of truth table in which the map is made up of cells, and each term in this represents the min term or max term of the function. By this method, we can directly minimize the Boolean function without following various steps.

15) Name the two forms of Boolean expression?

The two forms of Boolean expression are:

Sum of products (SOP) form.

The Product of sum (POS) form.

16) What are Minterm and Maxterm?

A minterm is called Product of sum because they are the logical AND of the set of variables and Maxterm are called sum of product because they are the logical OR of the set of variables.

17) Write down the Characteristics of Digital ICs?

The characteristics of digital ICs are -

Propagation delay.

Power Dissipation.

Fan-in.

Fan-out.

Noise Margin.

18) What are the limitations of the Karnaugh Map?

The limitations of Karnaugh Map are as follows:

It is limited to six variable maps which means more than six variable involving expressions are not reduced.

These are useful for only simplifying Boolean expression which is represented I standard form.

22) Define Fan-in and Fan-out?

Fan-in- The Fan-in of the gate means that the number of inputs that are connected to the gate without the degradation of the voltage level of the system.

Fan-out- The Fan-out is the maximum number of same inputs of the same IC family that a gate can drive maintaining its output levels within the specified limits.

23) Write the definition of the Duality Theorem?

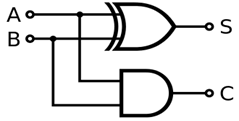
Duality Theorem states that we can derive another Boolean expression with the existing Boolean expression by:

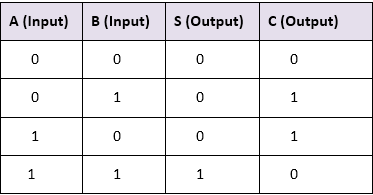
Changing OR operation (+ Sign) to AND operation (. Dot Sign) and vice versa.

Complimenting 0 and 1 in the expression by changing 0 to 1 and 1 to 0 respectively.

24) What is Half-Adder?

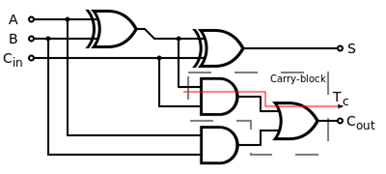
Half-adder is the circuits that perform the addition of two bits. It has two inputs A and B and two outputs S (sum) and C (carry). It is represented by XOR logic gate and an AND logic gate.

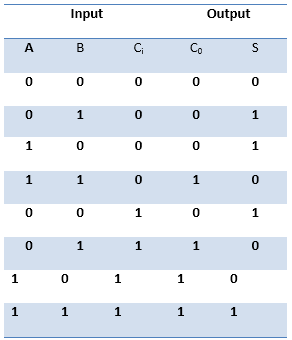




25) What is Full-Adder?

Full-adder is the circuits that perform the addition of three bits. It has three inputs A, B and a carry bit. Full adders are represented with AND, OR and XOR logic gate.





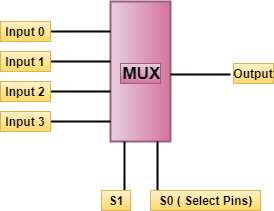
26) What is power dissipation?

Period time is the electrical energy used by the logic circuits. It is expressed in milliwatts or nanowatts.

Power dissipation = Supply voltage \* mean current taken from the supply.

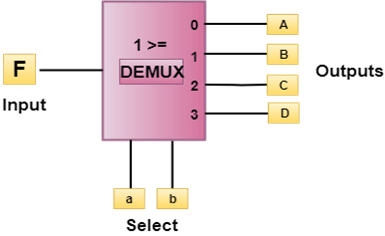
27) What is a Multiplexer?

The multiplexer is a digital switch which combines all the digital information from several sources and gives one output.



29) What is a Demultiplexer?

The demultiplexer is a circuit that receives the input on a single line and transmits this onto 2n possible output line. A Demultiplexer of 2n outputs has n select lines, which are used to select which output line is to be sent to the input. The demultiplexer is also called as Data Distributor.



30) What are the applications of Demultiplexer?

The applications of the demultiplexer are as follows:

It is used in the data transmission system with error detection.

It is used as a decoder for the conversion of binary to decimal.

It is used as a serial to parallel converter.

31) What are the differences between Combinational Circuits and Sequential Circuits?

The differences between combinational and sequential circuits are as follows:

S.No Combinational Circuits Sequential Circuits

1. These are faster in speed. These are slower.

2. These are easy to design. These are difficult to design.

3. The clock input is not required. The clock input is required.

4. In this, the memory units are not required. In this, the memory units are required to store the

previous values of inputs.

5. Example: Mux, Demux, encoder, decoder, Example: Shift registers, counters.

adders, subtractors.

32) Define Rise Time?

Rise time is the time that is required to change the voltage level from 10% to 90%.

33) Define fall time?

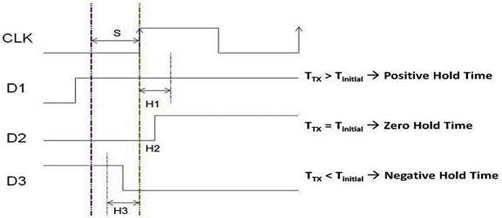
Fall time is the time that is required to change the voltage level from 90% to 10%.

34) Define Setup time?

The minimum time that is required to maintain the constant voltage levels at the excitation inputs of the flip-flop device before the triggering edge of the clock pulse for the levels to be reliably clocked in the flip flop is called the Setup time. It is denoted as tsetup.

35) Define Hold time?

The minimum time at which the voltage level becomes constant after triggering the clock pulse in order to reliably clock into the flip flop is called the Hold time. It is denoted by thold.



36) What is the difference between Synchronous and Asynchronous Counters?

The difference between Synchronous and Asynchronous Counters are as follows:

S.No Asynchronous Counters Synchronous Counters

1. These are low-speed Counters. These are high-speed Counters.

2. The Flip flops of these counters are not In these counters, the flip-flops are clocked

clocked simultaneously. simultaneously.

3. Simple logic circuits are there for more number of states. Complex logic circuits are there when the

number of states increases.

37) What are the applications of Flip-Flops?

The applications of flip-flops are:

Flip-flops are used as the delay element.

These are used for Data transfer.

Flip-flops are used in Frequency Division and Counting.

Flip-Flops are used as the memory element.

38) What is the difference between D-latch and D Flip-flop?

D-latch is level sensitive whereas flip-flop is edge sensitive. Flip-flops are made up of latches.

39) What are the applications of Buffer?

Applications of buffer are as follows:

Buffer helps to introduce small delays.

Buffer helps for high Fan-out.

Buffer are used to eliminate cross talks.

Q.2. What is the difference between digital system and analog system?

Answer: A digital system is a combination of devices designed to manipulate logical information or physical quantities that are represented in digital form that is the quantities can take only discrete values.

Example of digital systems includes digital computers and calculators, digital audio and video equipments etc.

An analog system contains devices that manipulate physical quantities that are represented in analog forms. In an analog system, the quantities can vary over a continuous range of values.

Q.4. What are the advantages of digital signal?

Answer: Advantages of digital signal are: Digital signals can be processed and transmitted more efficiently and reliably than analog signals. It is possible to store the digital data. Play back or further processing of the digital data is possible. The effect of noise (unwanted voltage fluctuations) is less. So digital data does not get corrupt.

Q.8. Which code is called as minimum change code and why?

Answer: Gray code is called as minimum change code because it has a very special feature that only one bit will change, each time the decimal number is incremented.

Q.11. What is the advantage of floating point representation compared to fixed point representation?

Answer: Quantization error is small and dynamic range is high for floating point representation so it is suitable for frequency domain algorithm.

Q.19. What is the difference between static logic circuits and dynamic logic circuits?

Answer: Static logic circuits perform the logical operations with voltage levels while dynamic logic circuits are based on the capacitive nature of input of MOSFET, working by transferring stored charges corresponding to logic levels from one circuit to another with the help of clock signals.

.20. Why look ahead carry adder is faster than ripple adder?

Answer: Look ahead carry adder is faster; since carry is generated in parallel at all the stages of addition rather than sequentially as in ripple adder.

27. Define memory word.

Answer: Memory word is a group of bits in a memory that represents instructions of some type. For example, a register consisting of 8 flip flops can be used as a memory for storing an 8 bit word.

28. What is direct memory access (DMA)?

Answer: DMA interface is used for transferring data directly between an external device and memory. The bus buffers in the microprocessor are disabled and go into a high impedance state during DMA transfer.

29. What is PLD?

Answer: Programmable logic device (PLD) is an IC that contains a large number of interconnected logic functions. The user can program the IC for a specific function by selective breaking the appropriate interconnections.

37. What are the characteristics of Metal Oxide Semiconductor logic (MOS)?

Answer: The characteristics of Metal Oxide Semiconductor logic (MOS) are-

MOS family uses negative logic for its operation.

It is very economical.

It is easier to make large complex chips.

It needs both positive and negative supplies.

Its speed is very low.

40. What is Fanout?

Answer: It is the maximum number of similar logic gate input that can be driven by a logic gate output without affecting the logic gate performance. High fanout is advantageous because it reduces the need for additional drivers to drive more gates.

41. What are combinational circuits?

Answer: A combinational circuit is a logic circuit the output of which depends only on the combination of the inputs. The output does not depend on the past values of inputs or outputs. Hence combinational circuits do not require any memory.

42. What is magnitude comparator?

Answer: A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitudes. The outcome of comparison is specified by three variables that indicates whether A>B, A<B or A=B.

44. Which saturated logic family is suitable for large scale integration (LSI)?

Answer: Integrated Injection logic (IIL) is the only saturated bipolar logic suitable for large scale integration because of small silicon chip area required and low power consumption.

47. What are sequential circuits?

Answer: In the sequential circuit, the timing parameter comes into picture. The output of a sequential circuit depends on the present time inputs, the previous output and the sequence in which the inputs are applied. In order to provide the previous input or output, a memory element is required to be used. Thus a sequential circuit needs a memory element.

48. How will you define the present state and next state of sequential circuit?

Answer: Present state- The data stored by the memory element at any given instant of time is called as the present state of the sequential circuit.

Next state- The combinational circuit operates on the external inputs and the present state to produce new outputs. Some of these new outputs are stored in the memory element and called as the next state of the sequential circuit.

7. Tell Some Of Applications Of Buffer?

Answer :

a) They are used to introduce small delays.

b) They are used to eliminate cross talk caused due to inter electrode capacitance due to close routing.

c) They are used to support high fan-out, e.g.: bufg

8. Give Two Ways Of Converting A Two Input Nand Gate To An Inverter?

Answer :

a) Short the 2 inputs of the nand gate and apply the single input to it.

b) Connect the output to one of the input and the other to the input signal.

9. Why Is Most Interrupts Active Low?

Answer :

This answers why most signals are active low if you consider the transistor level of a module, active low means the capacitor in the output terminal gets charged or discharged based on low to high and high to low transition respectively. When it goes from high to low it depends on the pull down resistor that pulls it down and it is relatively easy for the output capacitance to discharge rather than charging. Hence people prefer using active low signals.

12. Given The Following Fifo And Rules, How Deep Does The Fifo Need To Be To Prevent Underflow Or Overflow?

Answer :

RULES:

1) frequency(clk\_A) = frequency(clk\_B) / 4

2) period(en\_B) = period(clk\_A) \* 100

3) duty cycle(en\_B) = 25%

Assume clk\_B = 100MHz (10ns)

From (1), clk\_A = 25MHz (40ns)

From (2), period(en\_B) = 40ns \* 400 = 4000ns, but we only output for 1000ns,due to (3), so 3000ns of the enable we are doing no output work. Therefore, FIFO size = 3000ns/40ns = 75 entries

13. Differences Between D-latch And D Flip-flop?

Answer :

D-latch is level sensitive where as flip-flop is edge sensitive. Flip-flops are made up of latches.

15. What Are Set Up Time & Hold Time Constraints? What Do They Signify? Which One Is Critical For Estimating Maximum Clock Frequency Of A Circuit?

Answer :

Set up time is the amount of time the data should be stable before the application of the clock signal, where as the hold time is the amount of time the data should be stable after the application of the clock. Setup time signifies maximum delay constraints; hold time is for minimum delay constraints. Setup time is critical for establishing the maximum clock frequency.

16. How Can You Convert An Sr Flip-flop To A Jk Flip-flop?

Answer :

By giving the feedback we can convert, i.e. !Q=>S and Q=>R.Hence the S and R inputs will act as J and K respectively.

17. How Can You Convert The Jk Flip-flop To A D Flip-flop?

Answer :

By connecting the J input to the K through the inverter.

18. How Do You Detect If Two 8-bit Signals Are Same?

Answer :

XOR each bits of A with B (for e.g. A [0] xor B [0]) and so on. The o/p of 8 xor gates is then given as i/p to an 8-i/p nor gate.

if o/p is 1 then A=B.

19. Convert D-ff Into Divide By 2. (not Latch) What Is The Max Clock Frequency The Circuit Can Handle, Given The Following Information?

Answer :

T\_setup= 6nsT\_hold = 2nS T\_propagation = 10nS

Circuit: Connect Qbar to D and apply the clk at clk of DFF and take the O/P at Q. It gives freq/2. Max. Freq of operation: 1/ (propagation delay+setup time) = 1/16ns = 62.5 MHz

20. 7 Bit Ring Counter's Initial State Is 0100010. After How Many Clock Cycles Will It Return To The Initial State?

Answer :

6 cycles

21. Design All The Gates (not, And, Or, Nand, Nor, Xor, Xnor) Using 2:1 Multiplexer?

Answer :

Using 2:1 Mux, (2 inputs, 1 output and a select line)

a) NOT :Give the input at the select line and connect I0 to 1 & I1 to 0. So if A is 1, we will get I1 that is 0 at the O/P.

b) AND: Give input A at the select line and 0 to I0 and B to I1. O/p is A & B

c) OR: Give input A at the select line and 1 to I1 and B to I0. O/p will be A | B

d) NAND: AND + NOT implementations together

e) NOR: OR + NOT implementations together

f) XOR: A at the select line B at I0 and ~B at I1. ~B can be obtained from (a)

g) XNOR: A at the select line B at I1 and ~B at I0

22. Design A Circuit That Calculates The Square Of A Number?

Answer :

It should not use any multiplier circuits. It should use Multiplexers and other logic?

1^2=0+1=1

2^2=1+3=4

3^2=4+5=9

4^2=9+7=16

5^2=16+9=25

See a pattern yet? To get the next square, all you have to do is add the next odd number to the previous square that you found. See how 1,3,5,7 and finally 9 are added. Wouldn’t this be a possible solution to your question since it only will use a counter, multiplexer and a couple of adders? It seems it would take n clock cycles to calculate square of n.

24. What Is Race-around Problem? How Can You Rectify It?

Answer :

The clock pulse that remains in the 1 state while both J and K are equal to 1 will cause the output to complement again and repeat complementing until the pulse goes back to 0, this is called the race around problem. To avoid this undesirable operation, the clock pulse must have a time duration that is shorter than the propagation delay time of the F-F, this is restrictive so the alternative is master-slave or edge-triggered construction.

26. How Will You Implement A Full Subtractor From A Full Adder?

Answer :

All the bits of subtrahend should be connected to the xor gate. Other input to the xor being one. The input carry bit to the full adder should be made 1. Then the full adder works like a full subtract.

28. In A 3-bit Johnson's Counter What Are The Unused States?

Answer :

2(power n)-2n is the one used to find the unused states in Johnson counter.

So for a 3-bit counter it is 8-6=2.Unused states=2. the two unused states are 010 and 101.

29. What Is Difference Between Ram And Fifo?

Answer :

FIFO does not have address lines

Ram is used for storage purpose where as FIFO is used for synchronization purpose i.e. when two peripherals are working in different clock domains then we will go for FIFO.

30. Consider Two Similar Processors, One With A Clock Skew Of 100ps And Other With A Clock Skew Of 50ps. Which One Is Likely To Have More Power? Why?

Answer :

Clock skew of 50ps is more likely to have clock power. This is because it is likely that low-skew processor has better designed clock tree with more powerful and number of buffers and overheads to make skew better.

33. You Have Two Counters Counting Upto 16, Built From Negedge Dff , First Circuit Is Synchronous And Second Is "ripple" (cascading), Which Circuit Has A Less Propagation Delay? Why?

Answer :

The synchronous counter will have lesser delay as the input to each flop is readily available before the clock edge. Whereas the cascade counter will take long time as the output of one flop is used as clock to the other. So the delay will be propagating. For E.g.: 16 state counter = 4 bit counter = 4 Flip flops Let 10ns be the delay of each flop The worst case delay of ripple counter = 10 \* 4 = 40ns The delay of synchronous counter = 10ns only.(Delay of 1 flop)

34. Difference Between Synchronous And Asynchronous Reset?

Answer :

Synchronous reset logic will synthesize to smaller flip-flops, particularly if the reset is gated with the logic generating the dinput. But in such a case, the combinational logic gate count grows, so the overall gate count savings may not be that significant. The clock works as a filter for small reset glitches; however, if these glitches occur near the active clock edge, the Flip-flop could go metastable. In some designs, the reset must be generated by a set of internal conditions. A synchronous reset is recommended for these types of designs because it will filter the logic equation glitches between clocks.

Disadvantages of synchronous reset:

Problem with synchronous resets is that the synthesis tool cannot easily distinguish the reset signal from any other data signal. Synchronous resets may need a pulse stretcher to guarantee a reset pulse width wide enough to ensure reset is present during an active edge of the clock. if you have a gated clock to save power, the clock may be disabled coincident with the assertion of reset. Only an asynchronous reset will work in this situation, as the reset might be removed prior to the resumption of the clock. Designs that are pushing the limit for data path timing, cannot afford to have added gates and additional net delays in the data path due to logic inserted to handle synchronous resets.

Asynchronous reset:

The biggest problem with asynchronous resets is the reset release, also called reset removal. Using an asynchronous reset, the designer is guaranteed not to have the reset added to the data path. Another advantage favoring asynchronous resets is that the circuit can be reset with or without a clock present.

Disadvantages of asynchronous reset: ensure that the release of the reset can occur within one clock period. if the release of the reset occurred on or near a clock edge such that the flip-flops went metastable.

32. What are the characteristics of Resistor Transistor logic (RTL)?

Answer: The characteristics of Resistor Transistor logic (RTL)are-

Very much compatible with other logic families.

It is very economical. Its design is easy.

It has poor noise immunity.

Its speed is low.

Power dissipation is low.

It has low threshold and fan out is also less.

.35. What are the characteristics of Transistor Transistor logic (TTL)?

Answer: The characteristics of Transistor Transistor logic (TTL) are-

It has good current capability.

It is very economical.

Its switching speed is good.

It is compatible with DTL and CMOS.

Schottky type has very high switching speed and low power consumption.